

# 74AHC1G06; 74AHCT1G06

Inverter with open-drain output

Rev. 06 — 7 June 2007

Product data sheet

## 1. General description

74AHC1G06 and 74AHCT1G06 are high-speed Si-gate CMOS devices. They provide an inverting buffer. The output of these devices is an open-drain and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH, wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

## 2. Features

- High noise immunity
- Low power dissipation
- SOT353-1 and SOT753 package options
- ESD protection:
  - ◆ HBM JESD22-A114E: exceeds 2000 V
  - ◆ MM JESD22-A115-A: exceeds 200 V
  - ◆ CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

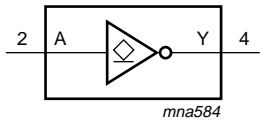
Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G06GW 74AHCT1G06GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G06GV 74AHCT1G06GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

## 4. Marking

**Table 2. Marking codes**

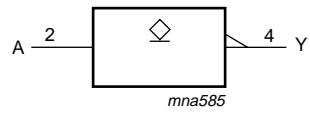
Type number	Marking
74AHC1G06GW	AR
74AHC1G06GV	A06
74AHCT1G06GW	CR
74AHCT1G06GV	C06

## 5. Functional diagram



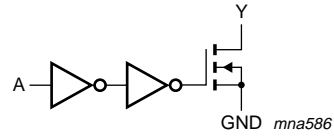
*mna584*

**Fig 1. Logic symbol**



*mna585*

**Fig 2. IEC logic symbol**



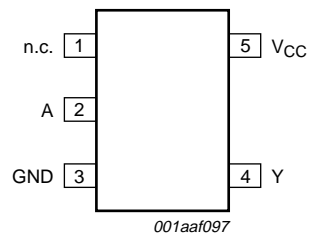
*mna586*

**Fig 3. Logic diagram**

## 6. Pinning information

### 6.1 Pinning

**74AHC1G06**  
**74AHCT1G06**



*001aaf097*

**Fig 4. Pin configuration**

### 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state*

Input	Output
A	Y
L	Z
H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V	[1] -	±20	mA
$I_O$	output current	$V_O > -0.5$ V	-	±25	mA
$V_O$	output voltage	active mode	[1] -0.5	+7.0	V
		high-impedance mode	[1] -0.5	+7.0	V
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	74AHC1G06			74AHCT1G06			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage	active mode	0	-	$V_{CC}$	0	-	$V_{CC}$	V
		high-impedance mode	0	-	6.0	0	-	6.0	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74AHC1G06</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	-	-	-	-	-	-	-	
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	20	μA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF
<b>For type 74AHCT1G06</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V	-	-	-	-	-	-	-	
		I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	20	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ . For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74AHC1G06</b>										
t <sub>PZL</sub>	OFF-state to LOW propagation delay	A to Y; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V <a href="#">[1]</a>								
		C <sub>L</sub> = 15 pF	-	3.7	7.0	1.0	7.7	1.0	8.1	ns
		C <sub>L</sub> = 50 pF	-	5.2	10.0	1.0	11.0	1.0	11.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <a href="#">[2]</a>								
		C <sub>L</sub> = 15 pF	-	2.7	4.9	1.0	5.3	1.0	5.6	ns
		C <sub>L</sub> = 50 pF	-	3.8	7.0	1.0	7.5	1.0	8.0	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	A to Y; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V <a href="#">[1]</a>								
		C <sub>L</sub> = 15 pF	-	4.8	6.4	1.0	6.9	1.0	7.4	ns
		C <sub>L</sub> = 50 pF	-	6.9	10.0	1.0	10.5	1.0	11.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <a href="#">[2]</a>								
		C <sub>L</sub> = 15 pF	-	3.0	4.1	1.0	4.6	1.0	5.1	ns
		C <sub>L</sub> = 50 pF	-	4.3	6.5	1.0	7.0	1.0	7.5	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; C <sub>L</sub> = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <a href="#">[3]</a>	-	3	-	-	-	-	-	pF
<b>For type 74AHCT1G06</b>										
t <sub>PZL</sub>	OFF-state to LOW propagation delay	A to Y; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 4.5 V to 5.5 V <a href="#">[2]</a>								
		C <sub>L</sub> = 15 pF	-	3.0	5.3	1.0	6.0	1.0	6.3	ns
		C <sub>L</sub> = 50 pF	-	4.2	7.5	1.0	8.5	1.0	9.0	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	A to Y; see <a href="#">Figure 5</a>								
		V <sub>CC</sub> = 4.5 V to 5.5 V <a href="#">[2]</a>								
		C <sub>L</sub> = 15 pF	-	3.2	4.6	1.0	5.1	1.0	5.6	ns
		C <sub>L</sub> = 50 pF	-	4.5	7.0	1.0	7.5	1.0	8.0	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; C <sub>L</sub> = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <a href="#">[3]</a>	-	4.5	-	-	-	-	-	pF

[1] Typical values are measured at V<sub>CC</sub> = 3.3 V.

[2] Typical values are measured at V<sub>CC</sub> = 5.0 V.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

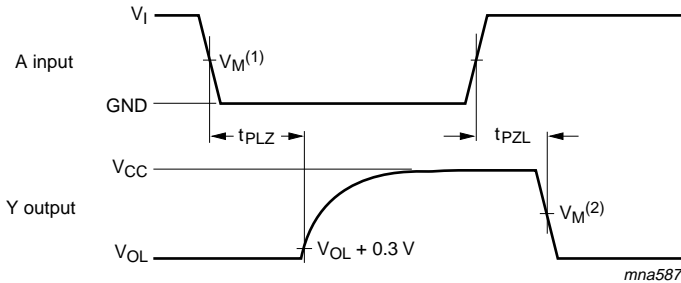
f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts

12. Waveforms

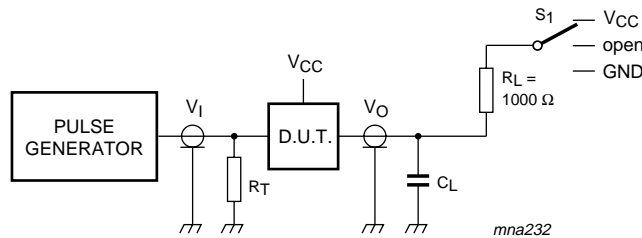


Measurement points are given in [Table 9](#).

Fig 5. Input (A) to output (Y) propagation delays

Table 9. Measurement point

Type	Input		Output
	$V_I$	$V_M^{(1)}$	$V_M^{(2)}$
74AHC1G06	GND to $V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT1G06	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 8](#). Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

For  $t_{PLZ}$ ,  $t_{PZH}$ ,  $S_1 = V_{CC}$

Fig 6. Load circuitry for switching times

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

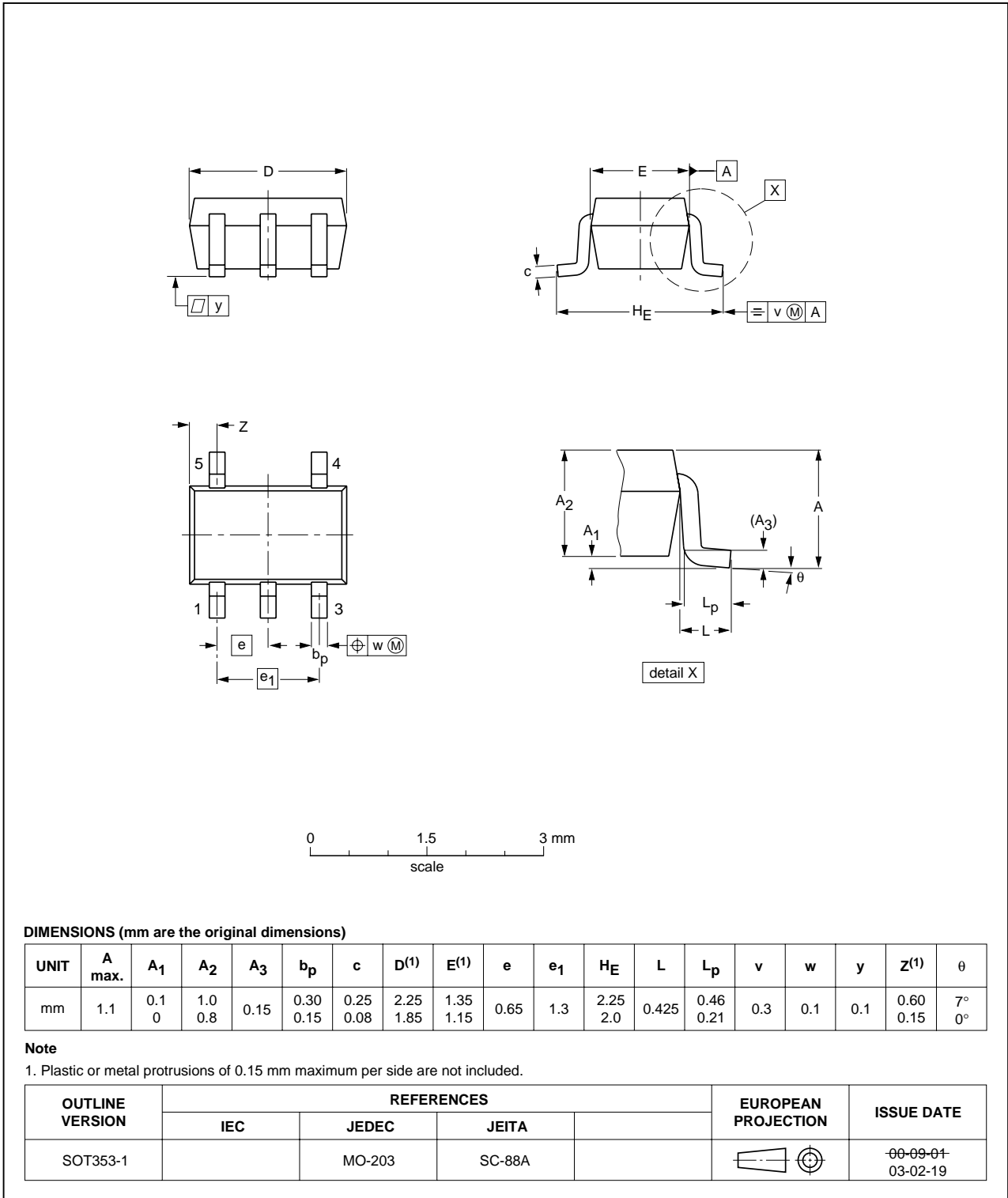


Fig 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

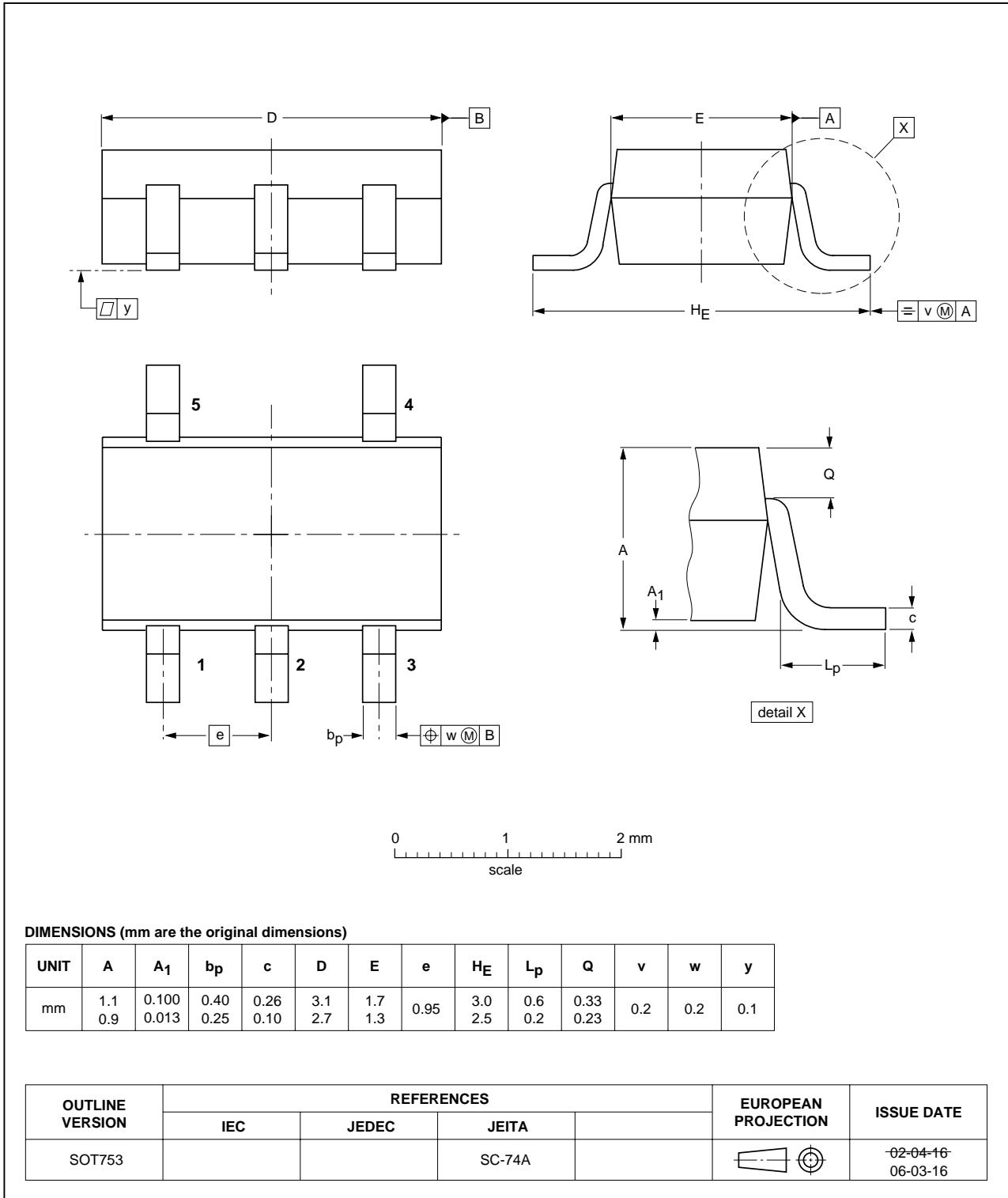


Fig 8. Package outline SOT753 (SC-74A)



## 14. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G06_6	20070607	Product data sheet	-	74AHC_AHCT1G06_5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Package SOT353 changed to SOT353-1 in <a href="#">Section 3</a> and <a href="#">Section 13</a>.</li> <li>Quick reference data and Soldering sections removed.</li> </ul>			
74AHC_AHCT1G06_5	20021002	Product specification	-	74AHC_AHCT1G06_4
74AHC_AHCT1G06_4	20020528	Product specification	-	74AHC_AHCT1G06_3
74AHC_AHCT1G06_3	20020221	Product specification	-	74AHC_AHCT1G06_2
74AHC_AHCT1G06_2	20010209	Product specification	-	74AHC_AHCT1G06_1
74AHC_AHCT1G06_1	20000501	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 7 June 2007

Document identifier: 74AHC\_AHCT1G06\_6